1. (Twice Amended) A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming oxide films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

masking said high-density region of said semiconductor substrate, and etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes;

uniformly forming a second nitride film having a predetermined thickness on the surface on which said first nitride film is etched;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing an assembly formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes reaching said semiconductor substrate in said interlayer insulating film, wherein portions of said second nitride film that are in direct contact with said first nitride film and that are positioned on at least one of the respective sides of said gate electrodes are removed as a result of the self-aligning step;

forming contact electrodes connected to said semiconductor substrate in said contact holes; and

annealing an assembly formed so far with a forming gas to recover an interfacial level.

6. (Twice Amended) A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming nitride protective films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

masking said high-density region of said semiconductor substrate, and etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes and also to expose said nitride protective films on said gate electrodes;

uniformly forming a second nitride film having a predetermined thickness on the surface on which said first nitride film is etched;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing an assembly formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes reaching said semiconductor substrate in said interlayer insulating film, wherein portions of said second nitride film that are in direct contact with said first nitride film and that are positioned on at least one of the respective sides of said gate electrodes are removed as a result of the self-aligning step;

forming contact electrodes connected to said semiconductor substrate in said contact holes; and

annealing an assembly formed so far with a forming gas to recover an interfacial level.

11. (Twice Amended) A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming oxide films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

masking said high-density region of said semiconductor substrate, and etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes;

C3

etching the exposed gate oxide film to expose said semiconductor substrate in the gaps between gate electrodes in said low-density region;

uniformly forming a second nitride film having a predetermined thickness on the surface on which said gate oxide film is etched;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing an assembly formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes reaching said semiconductor substrate in said interlayer insulating film, wherein portions of said second nitride film that are in direct contact with said first nitride film and that are positioned on at least one of the respective sides of said gate electrodes are removed as a result of the self-aligning step;

forming contact electrodes connected to said semiconductor substrate in said contact holes; and

annealing an assembly formed so far with a forming gas to recover an interfacial level.

18. (Twice Amended) A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming nitride protective films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes and also expose said nitride protective films on said gate electrodes;

C4

etching the exposed gate oxide film to expose said semiconductor substrate in the gaps between gate electrodes;

uniformly forming a second nitride film having a predetermined thickness on the surface on which said gate oxide film is etched;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing an assembly formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes reaching said semiconductor substrate in said interlayer insulating film, wherein portions of said second nitride film that are in direct contact with said first nitride film and that are positioned on at least one of the respective sides of said gate electrodes are removed as a result of the self-aligning step;

forming contact electrodes connected to said semiconductor substrate in said contact holes; and

C4 end

annealing an assembly formed so far with a forming gas to recover an interfacial level.

29. (Amended) A method according to claim 1, further comprising the step of:

a) planarizing a top surface of the interlayer insulating film; and

wherein the step of self-aligning said high-density region comprises the steps of:

b) forming an oxide film on the planarized top surface of the interlayer insulating film; and

c) in the high density region, masking the oxide film in a particular pattern using a fluorine-based resist,

C5

wherein the step a) is performed after the step of annealing in an atmosphere containing water vapor and before the step of self-aligning said high-density region.

30. (Amended) A method according to claim 6, further comprising the step of:

a) planarizing a top surface of the interlayer insulating film; and

wherein the step of self-aligning said high-density region comprises the steps of:

b) forming an oxide film on the planarized top surface of the interlayer insulating film; and

c) in the high density region, masking the oxide film in a particular pattern using a fluorine-based resist,

wherein the step a) is performed after the step of annealing in an atmosphere containing water vapor and before the step of self-aligning said high-density region.

31. (Amended) A method according to claim 11, further comprising the step of:

a) planarizing a top surface of the interlayer insulating film; and

wherein the step of self-aligning said high-density region comprises the steps of:

b) forming an oxide film on the planarized top surface of the interlayer insulating film; and

c) in the high density region, masking the oxide film in a particular pattern using a fluorine-based resist,

wherein the step a) is performed after the step of annealing in an atmosphere containing water vapor and before the step of self-aligning said high-density region.

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end

32. (Amended) A method according to claim 18, further comprising the step of:

a) planarizing a top surface of the interlayer insulating film; and

wherein the step of self-aligning said high-density region comprises the steps of:

b) forming an oxide film on the planarized top surface of the interlayer insulating film; and

c) in the high density region, masking the oxide film in a particular pattern using a fluorine-based resist,

wherein the step a) is performed after the step of annealing in an atmosphere containing water vapor and before the step of self-aligning said high-density region.